REMARKS

Claims 1-8 are pending in the application. Claims 6 and 7 are found to be allowable.

Applicant's claims 1 and 8 are amended to clarify that the counter means is synchronized with the input frame and the data read from memory 1 and input to memory 2 as the address is synchronized with the counter which is counting synchronized with the frames.

Claims 1-5 and 8 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishihara et al. (Ishihara). Reconsideration is respectfully requested for at least the following reasons:

The Office Action points to col. 9 and 10 of Ishihara which states the reading of the buffer memory 25 is started under control (enable control) of an output controller 27-5 in the timing of a state management table 27-6.

Specifically, since the timing is not received from the time slot counter 27-1, timing synchronization with an external frame is not made nor is it suggested in the cited reference.

This is in contrast the applicant's claimed invention, for example claim 8, where a counter counting ... in synchronization with the input frame, and outputting the count value as a read address and a write address.

This difference provides a disadvantage in Ishihara because the output is always accompanied by delay against a source signal (output in Figs. 7 and 9 (2)).

Because Ishihara teaches in col. 9: lines 55-57 that the write address controller 27 refers to the address management table 27 to generate the write addresses, thus the delay is apparent.

Ishihara fails to disclose a relationship with the counter with regard to address generation at the time of reading from the memory.

In contrast, according to applicant's claimed invention and as supported in applicant's specification, for example in the operation of memory 2 outputting a read address to be applied to memory 1, an output synchronous with a frame is obtained if the memory 2 applies the output of a counter synchronous with a frame to the memory 1.

Applicant's claimed invention provides the distinct advantage that the delay is reduced (in the case of handling signals of 64 kbps, the amount of delay in Figs. 2 and 6 is negligible).

Even if a header addition circuit is adopted in the reference, the number of parts of a circuit processing the input signals of one line as shown in Fig. 2 of the present invention is only three (four in Fig. 6). Therefore, applicant's claimed invention provides the advantage of a simpler circuit/control other that that as shown in the reference.

Also with regard to claim 1:

As taught by the reference and cited in the Office action at Col. 9, around lines 56 (1), the reference aims to dynamically assign the write address of a buffer memory 25, and a write address controller applies an address generated from the counter value of a time slot counter 27-1.

In contrast, applicant's claimed invention, in writing into memory 1 (Fig. 2), each piece of channel data is written into a position, synchronous with a frame signal since in writing, there is not need to dynamically assign a memory position.

Regarding claim 2:

The Office Action cites Ishihara col. 9, around lines 4 to 65 as teaching applicant's claim 2. This portion of the reference describes an address management table 27-4 in which a write address has a predetermined packet length (number of bits), and an address is generated by chaining a base address corresponding to the packet length (number of bits).

As seen in Figs. 7 and 9, the packet length is fixed, and an address is also chained in a predetermined fixed space. Therefore, the case where a packet length is variable is not considered nor suggested by Ishihara. This is contrary to applicant's claimed invention.

Applicant provides the bit length of one channel can be freely changed in a receiving frame during the operation of the apparatus, by rewriting mapping assigned to the memory 2.

Applicant's claim 2 recites: when a multiplexed line signal having an input frame of n bits per channel is processed, a time slot number of each bit of an n-bit channel is assigned to addresses of said first memory means, and data indicating switching information about a time slot of each piece of bit data is entered at each address of said second memory means.

The claimed invention may also include the case where the bit length of a specific channel is variable (if there are a variety of devices generating data to be inputted to the apparatus, even mixed signals can be handled. For example, a device A generates one channel of four bits, while a device B generates one channel of eight bits.).

The Office Action further recites Ishihara col. 14, around lines 30 to 40 which teaches, if in an overlap detection unit 79, a short cell maps across two ATM cells, a write address in which the short cell is stored in data memory 87 and its number of bytes (short cell length) are temporarily stored in overlap management memory 81, and on receipt of a time-divided cell, the two ATM cells are combined and output as one ATM cell.

The reference is teaching a process of writing a write address and its cell length (number of bytes) into management memory to combine two separated short cells. It is respectfully submitted that the relationship of this to the present claimed invention is not clear to the applicant.

Regarding claim 3:

The Ishihara is different from the claimed invention because it fails to disclose its selection conditions to be outputted from the controller 31.

Applicant's claim recites when a plurality of lines are accommodated by said cross-connection switch, any line of the plurality of lines is selected for a switching process by entering switching information about time order of data of a time slot and switching information data between lines at each address of said first memory means.

According to Ishihara col. 7, lines 15-35 as cited in the Office Action, the short cell assembly units 21-2 through 21-3 shown in Fig. 4 receives "13", "14" and "15" as selection signals from a controller 31 and a controller 27 generates "8", "9" and "10" each having a different timing. Thus, a selector 26 is controlled. This describes the combination process of each segment of data and a short cell header.

In the selection process of a selector 30 after this process, each segment of data is output as output line "7" after being selected by the selection signal from the controller 31. Thus the selection conditions to be output from the controller 31 are not described nor suggested by Ishihara.

According to the claimed invention as supported by the specification, the control of exchanging bits among input lines 1 through 8 shown in Fig. 6 is realized by rewriting the mapping of the memory 2. Therefore, unlike the reference, the cross connection function is realized without installing a controller at each level.

Regarding claim 4:

The Ishihara discloses at col. 10, lines 25-45, as referenced in the Office Action, a process of switching process of signals (input lines # 1 through #_) currently input in Fig. 12

(signals before a short cell addition process are switched and distributed among the short cell assembly units).

The reference discloses a process of switching currently input cell signals and transferring cells to a subsequent circuit (short cell assembly unit).

According to the present claimed invention, as supported in Figs. 8 and 14 of applicant's specification, the input data of the input line is always written into a time slot (address) corresponding to the frame.

As shown in figs. 7 and 10, in the cross-connection operation of channel bits, a bit exchange operation is realized by writing an exchange destination time slot number into an address indicating the target time slot of the memory 2.

In the case of Fig. 7, exchange destination "0100" is set in the address "0004" of the memory 2. In reality, as shown in Fig. 8, if the current time slot is channel 4, the data of exchange destination channel 100 is read.

In this case, since the channel 100 of a frame that is processing channel 4 is not inputted yet, then data of channel 100 written in the previous frame is read and is outputted to the time slot of channel 4.

In other words, applicant's claimed invention provides the advantage that the overall delay of a frame is reduced by inserting immediately previous frame data in a time slot.

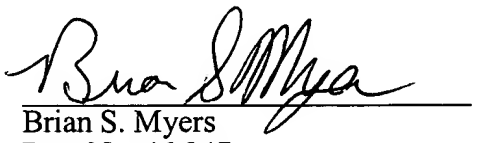
For at least the foregoing reasons it is respectfully requested the rejection of claims 1-4 be withdrawn. Claim 5 depends from claim 1 and is likewise in condition for allowance for at least the foregoing reasons.

Claim 8 is in condition for allowance for at least the same reasons set forth above with respect to claim 1 and for the additional distinguishing features.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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